EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	357	(712/214).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/07/03 10:21
L2	528	(712/215).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/07/03 10:28
L3	42	pipelin$3 near4 (floating?point or float$3) near4 exception$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/07/03 11:10
L4	121	pipelin$3 with (floating?point or float$3) with exception$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/07/03 12:27
L5	8	pipelin$3 with (floating?point or float$3) with exception$1 with latenc$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/07/03 11:13
L6	14	pipelin$3 same ((floating?point or float$3) with exception$1 with latenc$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/07/03 11:20
L7	30	pipelin$3 same ((floating?point or float$3) with latenc$3) same exception$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/07/03 11:27
L8	42	pipelin$3 same ((floating?point or float$3) same latenc$3) same exception$1	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/07/03 12:12
L9	3	pipelin$3 same ((floating?point or float$3) same latenc$3) same inhibit$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/07/03 12:12
L10	94	pipelin$3 same ((floating?point or float$3) same latenc$3) same stall$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/07/03 12:13
L11	7	pipelin$3 same ((floating?point or float$3) same latenc$3) same (stall$3 or bubble$1 or stop$4) same (exception$1 or interrupt$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/07/03 12:20

EAST Search History

L12	0	(pipelin$3 same ((floating?point or float$3) same latenc$3) same (exception$1 or interrupt$3)).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/07/03 12:21
L13	0	(((floating?point or float$3) same latenc$3) same (exception$1 or interrupt$3)).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/07/03 12:21
L14	0	((floating?point or float$3) same latenc$3 same exception$1 same (inhibit$3 or stall$3 or stop$5 or bubble$1)).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/07/03 12:22
L15	4	((floating?point or float$3) same exception$1 same (inhibit$3 or stall$3 or stop$5 or bubble$1)).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/07/03 12:22
L16	15	(pipelin$3 with (floating?point or float$3) with exception$1).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/07/03 12:28

Scholar All articles - Recent articles Results 1 - 10 of about 4,800 for (inhibit OR stall OR bubble) + (floating-point OR "floating point") + (exception OR interrupt)

All Results
Z Cvetanovic
D Anderson
D Bhandarkar
R Colwell
L Nguyen

Method and apparatus for **exception** handling in pipeline processors having mismatched instruction ... - all 2 versions »
DF Kinney, AN Drogaris, CH Mills, M Kahaiyan, J ... - US Patent 5,193,158, 1993 - Google Patents
... provoking instruction caused the processor to **inhibit** further instruction ... tion unit, or causes the **floating point** execution unit ... 60 to assume a **stall** condition ...
Cited by 35 - Related Articles - Web Search

Technique of incorporating **floating point** information into processor instructions - all 4 versions »
CC Hansen - US Patent 5,812,439, 1998 - Google Patents
... generate a system **stall** signal (which is coupled ... operands and predicts whether an **exception** will occur ... FPU 70 performs the **floating point** operation according to ...
Cited by 21 - Related Articles - Web Search

Method and apparatus for executing **floating point** (FP) instruction pairs in a pipelined processor by ... - all 3 versions »
D Avnon, HP Sharangpani, JB Sweedler - US Patent 5,559,977, 1996 - Google Patents
... In response to a pos -sible **exception**, the execution pipeline can **stall** the pipeline. The **floating-point** pipeline and the integer pipelines are stalled in an ...
Cited by 15 - Related Articles - Web Search

Qualification of register file write enables using self-timed **floating point exception** flags - all 2 versions »
RW Mason, ST Mangelsdorf - US Patent 5,257,214, 1993 - Google Patents
... may also include registersforstoring such **floatingpoint** ... and only goes high ("true") ifthere is no **floating point exception** which would **inhibit** the write ...
Cited by 14 - Related Articles - Web Search

A VLIW architecture for a trace scheduling compiler - all 15 versions »
RP Colwell, RP Nix, JJ O'Donnell, DB Papworth, PK ... - IEEE Transactions on Computers, 1988 - doi.ieeecs.org
... The **floating point** functional unit pipelines are "self- draining; " the destination register ... If a trap or **interrupt** occurs while the pipelined operation is ...
Cited by 379 - Related Articles - Web Search

Temporal re-alignment of a **floating point** pipeline to an integer pipeline for emulation of a load- ... - all 3 versions »
JS Blomgren, CS Brashears... - US Patent 5,884,057, 1999 - Google Patents
... The F4 stage can also **stall** if a ... **floatingpoint** pipeline 14 receives the floatingpointportion ... low. indicating CISC mode, stage PO of **floating point** ...
Cited by 4 - Related Articles - Web Search

[BOOK] Specification of Hazards, Stalls, Interrupts, and Exceptions in EXPRESSION - all 3 versions »
P Mishra, N Dutt, A Nicolau - 2001 - ics.uci.edu
... hazards leads to different kinds of stalls viz., pipe **stall**, unit **stall**, global **stall** etc. ... unusable, **floating-point exception** 14. ... 20. **Interrupt** (lowest priority ...
Cited by 3 - Related Articles - View as HTML - Web Search - Library Search

In-Order Issue Out-of-Order Execution **Floating-Point** Coprocessor for CalmRISC32 - all 4 versions »
K Seoul, SE Co, K Yong-In, K Seoul - doi.ieeecs.org
... generates appropriate control signals to **stall** the host ... is composed of a **floating-point** addition/subtraction unit, comparison unit and **exception** prediction ...
Cited by 2 - Related Articles - Web Search

Characterization of Alpha AXP performance using TP and SPECworkloads - all 3 versions »
Z Cvetanovic, D Bhandarkar - Computer Architecture, 1994. Proceedings the 21st Annual ..., 1994 - ieeexplore.ieee.org
... only a few percent (Compress is an **exception** with 13 ... are also pronounced in several **floating-point** SPEC benchmarks ... Figure 4). • The pipeline **stall** time varies ...
Cited by 73 - Related Articles - Web Search - BL Direct

Parallel processing type processor system with trap and stall control functions - all 3 versions »
T Aikawa, M Saito, K Minagawa, K Takeda - US Patent 5,561,774, 1996 - Google Patents
... ABSTRACT Aparallel processing type processor system with trap and **stall** control functions ... processor units are controlled such that when an **exception** is caused ...
Cited by 1 - Related Articles - Web Search

Scholar All articles - Recent articles Results 1 - 10 of about 2,020 for (inhibit OR stall OR bubble) + (floating-point OR "floating point") + (exception OR interrupt)

All Results
H Sharangpani
Z Cvetanovic
S Mirapuri
T Austin
G Chrysos

Method and apparatus for executing floating point (FP) instruction pairs in a pipelined processor by ... - all 3 versions »
D Avnon, HP Sharangpani, JB Sweedler - US Patent 5,559,977, 1996 - Google Patents
... as well, when the handling of the **exception** indicates that ... **latency** in the execution of the **floating-point** opera- tions ... there is a need to **stall** the subsequent ...
Cited by 15 - Related Articles - Web Search

An area-efficient standard-cell **floating-point** unit design for a processing-in-memory system - all 6 versions »
JS Moon, TJ Kwon, J Sondeen, J Draper - Solid-State Circuits Conference, 2003. ESSCIRC'03. ..., 2003 - ieeexplore.ieee.org
... For Int2Fp (Integer to **floating-point**) instruction, the fraction ... follows a divide instruction, a **pipeline stall** for seven ... in Verilog with the **exception** of the ...
Cited by 12 - Related Articles - Web Search

Temporal re-alignment of a **floating point pipeline** to an integer **pipeline** for emulation of a load- ... - all 3 versions »
JS Blomgren, CS Brashears... - US Patent 5,884,057, 1999 - Google Patents
... **Floating point** operands require specialized **floatingpoint** hardware which is located ... back to **floating point** register in stage F5 ... The F4 stage can also **stall** if a ...
Cited by 4 - Related Articles - Web Search

Method and apparatus for retarting **pipeline** processing - all 2 versions »
S Mirapuri, TJ Riordan... - US Patent 5,590,294, 1996 - Google Patents
... After the **exception** is processed, the processor returns ... processor state machine redefines the **stall** state based ... unit **14**, a **64-bit floating point** co-processor 16 ...
Cited by 18 - Related Articles - Web Search

In-Order Issue Out-of-Order Execution **Floating-Point** Coprocessor for CalmRISC32 - all 4 versions »
K Seoul, SE Co, K Yong-In, K Seoul - doi.ieeecs.org
... or more control signals from the host processor goes low to **stall** a coprocessor ... **Exception** prediction is the checking of the **floating- point** operation result ...
Cited by 2 - Related Articles - Web Search

Intel® Itanium™ Processor Microarchitecture Overview - all 27 versions »
H Sharangpani - Microprocessor Forum, 1999 - dig64.org
... High performance for commercial servers – Supercomputer-level **floating point** for technical workstations ... Fetch **bubble** Feed ... **Stall** Spill/Fill Injection ...
Cited by 15 - Related Articles - View as HTML - Web Search

Technique of incorporating **floating point** information into processor instructions - all 4 versions »
CC Hansen - US Patent 5,812,439, 1998 - Google Patents
... generate a system **stall** signal (which is coupled ... operands and predicts whether an **exception** will occur ... FPU 70 performs the **floating point** operation according to ...
Cited by 21 - Related Articles - Web Search

[BOOK] Protocol **Latency**: MIPS and Reality - all 10 versions »
D Mosberger, LL Peterson, S WO'Malley - 1995 - cs.arizona.edu
... as well as on processor **stall** rates. ... branch delay-slot or **pipeline** drain for **exception**. ... **Floating-point** instruction: Counts number of **floating-point** instruction ...
Cited by 28 - Related Articles - View as HTML - Web Search - Library Search

In order issue out-of-order execution **floating-point** coprocessorfor CalmRISC32
CH Jeong, WC Park, TD Han, SW Kim, MK Lee - Computer Arithmetic, 2001. Proceedings. 15th IEEE Symposium ..., 2001 - ieeexplore.ieee.org
... or more control signals from the host processor goes low to **stall** a coprocessor ... **Exception** prediction is the checking of the **floating- point** operation result ...
Related Articles - Web Search

The design and implementation of CalmRISC32 **floating point** unit - all 2 versions »
CH Jeong, WC Park, SW Kim, TD Han - ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE ..., 2000 - ieeexplore.ieee.org
... appropriate control signals to **stall** host processor ... ALU **pipeline** is composed of **floating-point** addition/subtraction ... comparison unit and **exception** pre- diction ...
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